

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of Miyano

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For DLL CIRCUIT

Box Non-Fee Amendment
Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified patent application as follows:

In the Specification:

Please substitute the following two paragraphs for the one paragraph beginning on line 25 of page 9:

Fig. 7 is a diagram illustrating a DLL circuit according to a first preferred embodiment of the invention including a schematic block diagram showing the construction of the DLL circuit.

Fig. 8 is a schematic block diagram showing the construction of bias generation means included in this DLL circuit.

Please substitute the following paragraph for the paragraph beginning on line 4 of page 10:

Fig. 9 is a diagram showing an embodiment of first and second bias generation circuits shown in Fig. 8.

Please substitute the following paragraph for the paragraph beginning on line 6 of page 10:

Fig. 10 is a circuit diagram showing an embodiment of counting control means shown in Fig. 8.

Please substitute the following two paragraphs for the one paragraph beginning on line 26 of page 10:

Fig. 7 is a diagram illustrating a DLL circuit according to a first preferred embodiment of the invention including a schematic block diagram showing the construction of a DLL circuit 100.

Fig. 8 is a schematic block diagram showing the construction of bias generation means 200 included in this DLL circuit 100.

Please substitute the following paragraph for the paragraph beginning on line 5 of page 11:

With reference to Fig. 7, the DLL circuit 100 according to this preferred embodiment comprises: phase shifting means 120 which, based on an input signal 300, generates, for example, 8 phase shifting processing signals 310 having phase differences at equal spacings (45 degrees); phase comparison means 140 which compares the phase of the input signal 300 with the phase of an output feedback signal 330 to detect a phase difference and, based on the detected phase difference, outputs a phase control signal 340; phase synthesizing means 160 which outputs a phase corrected signal 320 having a predetermined phase relationship with the input signals 300 based on the 8 phase shifting processing signals 310, generated by the phase shifting means 120, and the phase control signal 340; and first duty correction means 170 which corrects the duty of the phase corrected signal 320 to a predetermined duty (for example, 49 to 51%) and outputs a phase lock signal 400.

Please substitute the following paragraph for the paragraph beginning on line 4 of page 13:

Fig. 9 is a circuit diagram showing an embodiment of the first and second bias generation circuits 250, 270 shown in Fig. 8.

Please substitute the following paragraph for the paragraph beginning on line 8 of page 14:

All of each source electrode terminal of a group of current regulation PMOSs composed of 6 PMOSs 13 to 18, a drain electrode terminal of PMOS 19, and each gate electrode terminal of PMOSs 19, 20 are connected by common connection. Each source electrode terminal of PMOSs 19, 20 is connected to VDD. Each drain electrode terminal of the group of current regulation PMOSs and each drain electrode terminal of a group of current regulation NMOSs composed of 6 NMOSs 52 to 57 are connected by common connection in a combination of PMOS 13 with NMOS 52, a combination of PMOS 14 with NMOS 53, a combination of PMOS 15 with NMOS 54, a combination of PMOS 16 with NMOS 55, a combination of PMOS 17 with NMOS 56, and a combination of PMOS 18 with NMOS 57. Each gate electrode terminal of the group of current regulation NMOSs is connected to the output terminal 81 of the first bias generation circuit 250. Each source electrode terminal of the group of current regulation NMOSs is connected to GND. A drain electrode terminal of PMOS 20, a drain electrode terminal and a gate electrode terminal of NMOS 58, and an output terminal 82 of the second bias generation circuit 270 are connected by common connection. A source electrode terminal of NMOS 58 is connected to GND. Gate electrode terminals 13G to 18G of the group of current regulation PMOSs are connected respectively to corresponding output signal terminals of the correction signal generation means 216 shown in Fig. 8 so that bias correction signals 381 to 386 are input respectively into the gate electrode terminals 13G to 18G.

Please substitute the following paragraph for the paragraph beginning on line 6 of page 18:

Fig. 14 is a diagram illustrating major signals associated with the counting control means 220, wherein (a) represents a typical timing chart for the first counting control signal 304, (b) represents a typical timing chart for a potential Vct at the common connection point 91, (c) represents a typical timing chart for the second counting control signal 308, and (d) represents a typical timing chart of the counting result signal 370 in Fig. 8.

Please substitute the following paragraph for the paragraph beginning on line 19 of page 20:

Next, the operation of the bias generation means 200, which is a feature of the invention, will be explained in conjunction with Figs. 7 to 11 and 14.

Please insert the following before the paragraph beginning on line 19 of page 32:

REFERENCES IN FIGURES

FIGURE 1:

- 511 PHASE DECISION CIRCUIT
- 513 LEVEL SHIFTING CIRCUIT
- 541 4-PHASE BASIC CLOCK GENERATION CIRCUIT
- 542 PHASE DETECTION CIRCUIT
- 543 PHASE SHIFTING CIRCUIT
- 544 PHASE REGULATION DECISION CIRCUIT
- 545 OUTPUT CIRCUIT
- 601 OUTPUT CLOCK
- 602 REFERENCE CLOCK
- 603 OUTPUT CLOCK
- 608, 609 CONTROL SIGNAL
- 610 - 617 SIGNAL

FIGURE 2:

723 MUX (MULTIPLEXOR)

FIGURE 3:

810 PHASE DETECTOR

811 - 814 P-CHANNEL TRANSISTOR

815, 816 NODE

817, 818 CAPACITOR

819, 820, 821 N-CHANNEL TRANSISTOR

822 TRANSISTOR

823 NODE

824 CURRENT SOURCE

825 PARASITIC CAPACITY

839 COMPARATOR

 V_{IN1} INPUT SIGNAL V_{IN2} INPUT SIGNAL V_{DD} POWER TERMINAL V_{EQ} EQUALIZATION SIGNAL V_{REF} REFERENCE VOLTAGE

FIGURE 4:

M1 - M10 TRANSISTOR

910, 915 UNCORRECTED INPUT SIGNAL

920, 925 ERROR VALUE

930, 940 BIAS CURRENT

950, 955 CORRECTED DIFFERENTIAL CLOCK SIGNAL

960, 965 INVERTER

970, 975 NODE

GND GROUND TERMINAL

 V_{DD} POWER TERMINAL

FIGURE 5:

1560 PHASE SHIFTER
 1565 REFERENCE CLOCK
 1573 CONSTANT-CURRENT SUPPLY LINE
 1575 SIGNAL LINE
 1577 RESULT OF PHASE DECISION
 1585 PHASE SELECT SIGNAL
 1587 OUTPUT CLOCK

FIGURE 6:

1501 CURRENT SOURCE
 1502, 1503 DIFFERENTIAL N-CHANNEL FIELD-EFFECT TRANSISTOR (FET)
 1504, 1505 FIXED CURRENT SOURCE
 1506, 1507 BRANCH
 1515, 1525 SIGNAL LINE
 1550 PHASE MIXER
 1590, 1595 CAPACITOR
 1596 AMPLIFIER

FIGURE 7:

100 DLL CIRCUIT
 310 PHASE SHIFTING PROCESSING SIGNAL
 320 PHASE CORRECTED SIGNAL
 330 FEEDBACK SIGNAL
 340 PHASE CONTROL SIGNAL
 390 BIAS SIGNAL

FIGURE 8:

302 TRIGGER SIGNAL
 304, 305, 306 FIRST COUNTING CONTROL SIGNAL

308 SECOND COUNTING CONTROL SIGNAL
 370 COUNTING RESULT SIGNAL
 380 BIAS CORRECTION SIGNAL
 392 PRIMARY BIAS SIGNAL
 395 INTERNAL BIAS SIGNAL

FIGURE 9:

1 RESISTIVE ELEMENT
 2 DIODE
 11 - 20 PMOS (P-CHANNEL MOS)
 I1 - I6 CURRENT VALUE
 13G - 18G ELECTRODE TERMINAL
 Is1 CURRENT VALUE
 Is2 CURRENT VALUE
 51 - 58 NMOS (N-CHANNEL MOS)
 81, 82, OUTPUT TERMINAL
 250 FIRST BIAS GENERATION CIRCUIT
 270 SECOND BIAS GENERATION CIRCUIT
 380 BIAS CORRECTION SIGNAL
 381 - 386 CORRECTION SIGNAL
 392 PRIMARY BIAS SIGNAL
 395 INTERNAL BIAS SIGNAL
 GND GROUND TERMINAL
 VDD POWER TERMINAL

FIGURE 10:

5 CAPACITATIVE ELEMENT
 10 COMPARISON CIRCUIT
 21 PMOS (P-CHANNEL MOS)
 61 FIRST NMOS
 62 SECOND NMOS

62G GATE ELECTRODE TERMINAL
 83 FIRST INPUT TERMINAL
 84 SECOND INPUT TERMINAL
 85 OUTPUT TERMINAL
 91 COMMON CONNECTION
 92 COMMON CONNECTION
 220 COUNTING CONTROL MEANS
 304 FIRST COUNTING CONTROL SIGNAL
 308 SECOND COUNTING CONTROL SIGNAL
 392 PRIMARY BIAS SIGNAL
 GND GROUND TERMINAL
 VDD POWER TERMINAL
 Vref POTENTIAL

FIGURE 11A:

214 COUNTING CIRCUIT
 300 INPUT SIGNAL
 305, 306 FIRST COUNTING CONTROL SIGNAL
 308 SECOND COUNTING CONTROL SIGNAL
 370 COUNTING RESULT SIGNAL
 371 - 376 OUTPUT BIT
 380 BIAS CORRECTION SIGNAL
 381 LEAST SIGNIFICANT BIT SIGNAL
 382 - 385 BIT SIGNAL
 386 MOST SIGNIFICANT BIT SIGNAL

FIGURE 12:

110 DLL CIRCUIT
 310 PHASE SHIFTING PROCESSING SIGNAL
 320 PHASE CORRECTED SIGNAL
 330 FEEDBACK SIGNAL

340 PHASE CONTROL SIGNAL

390 BIAS SIGNAL

FIGURE 13:

7, 8 RESISTIVE ELEMENT

31 FIRST PMOS

33 SECOND PMOS

35 THIRD PMOS

35G ELECTRODE TERMINAL

37 FOURTH PMOS

65, 66 NMOS

67 THIRD NMOS

68 FOURTH NMOS

69 FIFTH NMOS

71 NMOS

71G GATE ELECTRODE TERMINAL

72 NMOS

72G GATE ELECTRODE TERMINAL

73 SIXTH NMOS

73G GATE ELECTRODE TERMINAL

95 - 98 COMMON CONNECTION

190 FUNCTIONAL BLOCK

191 INTERNAL PROCESSOR

193 FINAL STAGE DIFFERENTIAL

AMPLIFIER CIRCUIT

195 LEVEL CONVERTER

197 SIGNAL OUTPUT SECTION

392 PRIMARY BIAS SIGNAL

395 INTERNAL BIAS SIGNAL

GND GROUND TERMINAL

VDD POWER TERMINAL

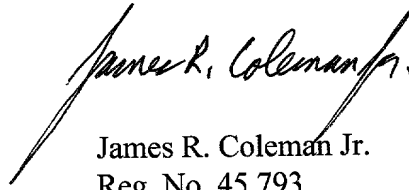
FIGURE 14:

304 FIRST COUNTING CONTROL SIGNAL

308 SECOND COUNTING CONTROL SIGNAL

370 COUNTING RESULT SIGNAL

Respectfully submitted,



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APPENDIX A MARKED-UP SPECIFICATION

Amendments to the paragraph beginning on line 25 of page 9:

Fig. [8] 7 is a diagram illustrating a DLL circuit according to a first preferred embodiment of the invention, [wherein Fig. 8A is] including a schematic block diagram showing the construction of the DLL [circuit,] circuit.

[and] Fig. [8B] 8 is a schematic block diagram showing the construction of bias generation means included in this DLL circuit.

Amendment of the paragraph beginning on line 4 of page 10:

Fig. 9 is a diagram showing an embodiment of first and second bias generation circuits shown in Fig. [8B] 8.

Amendment of the paragraph beginning on line 6 of page 10:

Fig. 10 is a circuit diagram showing an embodiment of counting control means shown in Fig. [8B] 8.

Amendment of the paragraph beginning on line 26 of page 10:

Fig. [8] 7 is a diagram illustrating a DLL circuit according to a first preferred embodiment of the invention[, wherein fig. 8A is] including a schematic block diagram showing the construction of a DLL circuit 100, [and] Fig. [8B] 8 is a schematic block diagram showing the construction of bias generation means 200 included in this DLL circuit 100.

Amendment of the paragraph beginning on line 5 of page 11.

With reference to Fig. [8] 7, the DLL circuit 100 according to this preferred embodiment comprises: phase shifting means 120 which, based on an input signal 300, generates, for example, 8 phase shifting processing

signals 310 having phase differences at equal spacings (45 degrees); phase comparison means 140 which compares the phase of the input signal 300 with the phase of an output feedback signal 330 to detect a phase difference and, based on the detected phase difference, outputs a phase control signal 340; phase synthesizing means 160 which outputs a phase corrected signal 320 having a predetermined phase relationship with the input signals 300 based on the 8 phase shifting processing signals 310, generated by the phase shifting means 120, and the phase control signal 340; and first duty correction means 170 which corrects the duty of the phase corrected signal 320 to a predetermined duty (for example, 49 to 51%) and outputs a phase lock signal 400.

Amend of the paragraph beginning on line 4 of page 13.

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Amendment of the paragraph beginning on line 8 of page 14.

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Amendment of the paragraph beginning on line 6 of page 18.

Fig. 14 is a diagram illustrating major signals associated with the counting control means 220, wherein (a) represents a typical timing chart for the first counting control signal 304, (b) represents a typical timing chart for a potential V_{ct} at the common connection point 91, (c) represents a typical timing chart for the second counting control signal 308, and (d) represents a typical timing chart of the counting result signal 370 in Fig. [8B] 8.

Amendment of the paragraph beginning on line 19 of page 20.

Next, the operation of the bias generation means 200, which is a feature of the invention, will be explained in conjunction with Figs. [8A] 7 to 11 and 14.